

CLAIMS

We claim:

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1. A complementary metal oxide semiconductor (CMOS) device with an integrated photosensitive junction field-effect transistor (JFET), the device comprising:
 - a silicon substrate;
 - a JFET formed on a surface of the silicon substrate, the JFET including a photo-absorbing layer formed on the surface of the silicon substrate; and
 - an overglass layer formed over the JFET adapted to admit photons to the photo-absorbing layer of the JFET,wherein the JFET detects incident photons admitted through the overglass layer and produces an amplified electrical signal corresponding to the photons detected.
 2. A CMOS device as in claim 1,
wherein the JFET provides a relatively low corner frequency.
 3. A CMOS device as in claim 1,
wherein an input referred noise of the JFET is relatively low.
 4. A CMOS active pixel sensor (APS) pixel supported on a substrate comprising:
 - a junction field-effect transistor (JFET) adapted to detect photons and produce an amplified electrical signal corresponding to the photons detected; and
 - a readout switch transistor coupled to a drain terminal of the JFET.

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5. A CMOS APS pixel as in claim 4,

wherein a source terminal of the readout switch transistor is connected to a bus and a resistor, forming a source follower circuit.

6. A CMOS APS pixel as in claim 4, further comprising:

a first resistor connected between a gate terminal of the JFET and a drain terminal of the readout switch transistor; and

a second resistor connected between a source terminal of the JFET and the drain terminal of the readout switch transistor, wherein the first and second resistors provide positive feedback and laser trimmability, and

wherein a source terminal of the readout switch transistor is connected to a bus and a current source, forming a source follower.

7. A CMOS APS pixel as in claim 4,

wherein the JFET is contained in a differential amplifier circuit.

8. A digital camera, comprising:

a CMOS active pixel sensor (APS) imager providing image data, the imager comprising:

an array of CMOS APS pixels comprising a plurality of junction field-effect transistors (JFETs) adapted for photodetection and electrical signal amplification.

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9. A digital camera as in claim 8, the array of CMOS APS pixels comprising:
a silicon substrate;
a JFET formed on the surface of the silicon substrate comprising:
a photo absorbing layer formed on a surface of the silicon substrate;
an overglass layer formed over the JFET adapted to admit photons to
the photo-absorbing layer of the JFET
wherein the JFET detects incident photons admitted through the overglass
layer and produces an amplified electrical signal corresponding to the photons
detected.

10. A digital camera as in claim 8, the CMOS APS pixels further comprising:
a readout switch transistor coupled to a drain terminal of the JFET.

11. A digital camera as in claim 10, wherein a source terminal of the readout
switch transistor is connected to a bus and a resistor, forming a source follower circuit.

12. A digital camera as in claim 10, wherein each JFET of the plurality of JFETs is
contained in a differential amplifier circuit.

13. A process of fabricating a CMOS integrated circuit device with JFETs on a
wafer of semiconductor material, the wafer including a substrate and a silicon wafer layer
thereon, the process comprising sequentially performing the steps of:

4 forming an active region on the silicon wafer layer;

5 forming an N-well region of predetermined depth in the silicon wafer layer;

6 forming a P-well region of predetermined depth in the silicon wafer layer;

7 depositing a field oxide layer on the n-well region;

8 implanting a dopant to form an N-channel of a desired threshold voltage in the

9 active region;

10 implanting a dopant to form a P-channel of a desired threshold voltage in the

11 active region;

12 depositing an oxide layer and a polysilicon layer on the wafer;

13 etching the polysilicon layer to form a CMOS gate in the active region;

14 forming a JFET area in the active region;

15 implanting a N lightly doped drain in the substrate;

16 implanting a P lightly doped drain in the substrate;

17 forming a lightly doped drain spacer in the substrate;

18 forming an n+ contact to the n-well;

19 forming an p+ contact to the p-well;

20 activating CMOS source and drain contacts for the CMOS gates;

21 salicidizing the wafer;

22 forming a tungsten plug in the CMOS integrated circuit device; and

23 forming a metal layer on the CMOS integrated circuit device.

1 14. A process as in claim 13, wherein the step of forming a JFET area comprises:
2 creating and implanting a channel in the JFET area;
3 depositing polysilicon and nitride layers for JFET gate formation on the JFET
4 area; and
5 forming a JFET gate in the JFET area.

1 *Bl* 15. A process as in claim 14, the step of depositing layers for JFET gate formation
2 *cont* comprising the steps of:

3 depositing a polysilicon layer on the JFET area;
4 implanting the polysilicon layer with boron difluoride ions; and
5 depositing a nitride layer on the polysilicon layer.

1 16. A process as in claim 14, the step of forming a JFET gate comprising the steps
2 of:

3 etching the nitride layer; and
4 etching the polysilicon layer.

1 17. A process as in claim 14, the step of creating and implanting a channel in the
2 JFET area comprising the step of:

3 depositing an oxide layer in the JFET area.

4 18. The process as in claim 14, the step of activating CMOS source and drain
5 contacts comprising the step of:
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removing the nitride layer in the JFET area.

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19. A process as in claim 13, further comprising the step of:

forming a CMOS APS imager from the CMOS integrated circuit device.

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